Abstract of the Disclosure

A power semiconductor device having high avalanche capability comprises an N^+ doped substrate and, in sequence, N^- doped, P^- doped, and P^+ doped semiconductor layers, the P^- and P^+ doped layers having a combined thickness of about 5 μm to about 12 μm. Recombination centers comprising noble metal impurities are disposed substantially in the N^- and P^- doped layers. A process for forming a power semiconductor device with high avalanche capability comprises: forming an N^- doped epitaxial layer on an N^+ doped substrate, forming a P^- doped layer in the N^- doped epitaxial layer, forming a P^+ doped layer in the P^- doped layer, and forming in the P^- and N^- doped layers recombination centers comprising noble metal impurities. The P^+ and P^- doped layers have a combined thickness of about 5 μm to about 12 μm.